REMARKS

Claims 1-6 and 17-29 are all the claims presently pending in the application.

Claims 7-16 have been canceled without prejudice or disclaimer as being directed to non-elected inventions.

Claims 1 and 3 have been amended to define more particularly the features of the present invention.

Claims 17-29 have been added to claim additional features of the invention.

No new matter is added.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claim 3 is rejected under 35 U.S.C. § 112, second paragraph.

With respect to the prior art rejections, claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Asami (U.S. Patent No. 4,750,027).

Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asami in view of Osono, et al. (JP 11-176941).

Claim 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asami in view of Applicants' allegedly Admitted Prior Art (AAPA).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

In conventional fabrication methods of semiconductor devices, wells are formed close to the wafer surface and impurities are injected into the wells to form diffusion layers. Thereafter trenches are formed in element isolation areas for isolating each element. An oxide film (insulating film) is then formed over the entire surface of the wafer including the interiors of the trenches. The wafer surface then is planarized so that the oxide film of the wafer surface is removed to expose the surface of the diffusion layers. Since polishing proceeds further in regions of the wafer surface having few diffusion layers than in areas having many diffusion layers, raising the problem of excessive abrasion of the wafer surface, there is a problem, however, that the amount of abrasion of the wafer surface differs depending on the distribution of the diffusion layers (e.g., see specification at page 1, lines 9-23).

A conventional method for creating a layout pattern of a semiconductor device involves arranging fill cells (also referred to as "dummy cells"), composed only of wells, in vacant areas that lack circuit patterns. In this conventional method, a semiconductor device is fabricated by making mask data from a layout pattern that includes fill cells, fabricating a reticle based on this mask data, and then forming diffusion layers or wiring layers by using the reticle. Nevertheless, such an arrangement of fill cells composed only of wells in vacant areas cannot solve the above-described problems in processing the wafer surface (e.g., see specification at page 1, lines 24-27, and page 2, lines 1-2).

In conventional methods, after creating the layout pattern of a semiconductor device, dummy data of diffusion layers are inserted in a mask data of areas having few diffusion layers when making mask data, whereby the distribution of diffusion layers is made uniform. However, the conventional methods in which dummy data are added to

the mask data when making mask data is problematic because the distribution of diffusion layers and the size of vacant areas must be calculated from the layout pattern, and this calculation entails complex arithmetic processes and an excessive amount of processing time (e.g., see specification at page 2, lines 3-20).

The claimed invention, on the other hand, provides a method and device for producing the layout pattern of a semiconductor device that enables uniform planarization of the wafer surface in the CMP processing carried out before forming transistors, and further, that enables a reduction of trouble of the arithmetic processes when producing mask data (e.g., see specification at page 3, lines 14-18).

For example, in dependent claim 1 exemplarily defines a method of producing a layout pattern of a semiconductor device, including arranging primitive cells including circuit patterns of constituent elements of the semiconductor device in an element formation area of the semiconductor device, and arranging at least one fill cell with a diffusion layer and no wiring, in a vacant area in the element formation area of the semiconductor device that is generated after the primitive cells associated with all constituent elements of the semiconductor device have been arranged.

It is noted that the specification clearly defines that a "*fill cell*", according to the exemplary aspects of the present invention, includes a construction without gate electrodes (e.g., see specification at page 7, lines 15-18).

According to the claimed invention, since the fill cells can be arranged so as to make the data ratio of the diffusion layer (area ratio of the diffusion layer) fall within a prescribed range, uneven distribution of the diffusion layers is eliminated, whereby a wafer having a uniform surface can be obtained even when CMP is conducted to remove the insulating film on a wafer having diffusion layers and trenches formed thereon.

Further, fill cells according to the exemplary aspects of the claimed invention can be arranged after primitive cells have been arranged and before mask data are made, and the arithmetic processes for making mask data can therefore be reduced (e.g., see specification at page 3, lines 24-27; page 4, lines 1-5; and page 14, lines 2-9).

The claimed invention also can reduce the trouble of the arrangement process of the fill cells and can prevent an increase in the amount of calculation when making mask data from a layout pattern. The claimed invention can shorten wiring between constituent elements, reduce the wiring capacitance, and obtain a semiconductor device that operates at higher speed (e.g., see specification at page 4, lines 6-23).

Finally, when arranging fill cells, the use of both unit fill cell and a variety of composite fill cells of combination of a plurality of unit fill cells enables the vacant areas that are generated after primitive cells have been arranged to be efficiently filled by fill cells. In addition, the use of the same amount of information to designate both unit fill cell and composite fill cell can prevent an increase in the amount of calculation when producing mask data from a layout pattern (e.g., see specification at page 14, lines 10-15).

II. 35 U.S.C. § 112 REJECTION

Claim 3 stands rejected under 35 U.S.C. 112, second paragraph, as being indefinite.

Particularly, the Examiner asserts that claim 3 recites "*said fill cells are arranged such that a distribution ratio falls within the range 30-55% in said element formation area, said distribution ration being the proportion of said diffusion layer that are distributed in said element formation area of said semiconductor device*"; the

independent claim 1 recites "arranging at least one fill cell with a diffusion layer and no wiring, in vacant area". The Examiner requests clarification.

Applicants submit that the ordinarily skilled artisan would clearly know and understand the meaning of claim 3, in view of the exemplary description of this feature in the specification (e.g., see specification at page 12, lines 15-23).

However, to speed prosecution, claim 3 is amended to define more clearly the features of the claimed invention, thereby overcoming this rejection. Applicant submits that the ordinarily skilled artisan would know and understand the scope of the claimed invention.

Therefore, the Examiner is requested to reconsider and withdraw this rejection.

Since claim 3 is not rejected on prior art grounds, Applicants submit that claim 3 should now be in condition for immediate allowance.

III. THE PRIOR ART REJECTIONS

A. Claims 1 and 2 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Asami. The Examiner alleges that Asami discloses all of the features of the claimed invention.

Particularly, the Examiner alleges that Asami shows a method of producing a layout pattern of a semiconductor device, comprising the steps of: arranging primitive cells having circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device; and arranging at least one fill cell with a diffusion layer and no wiring, in vacant area that is generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged (Abstract, Figs. 1-5B, 8-11, col. 2, lines 58-67, col. 3, lines 1-68, col. 4, lines 20-

50, col. 5, lines 1-68, col. 6, lines 3-30). The Examiner further alleges that Asami discloses the fill cells being arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device (Figs. 1-5B, 8-11). In addition, the Examiner notes that the elements must be arranged as required by the claim, but this is not an ipsissimis verbis test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990).

Applicants respectfully submit, however, that there are features of the claimed invention which are not disclosed or suggested by Asami. Therefore, Applicants traverse this rejection.

First, Applicants respectfully note that the Examiner has not identified which features of the Asami reference have been deemed to disclose or suggest the features of the claimed invention (e.g., see 37 C.F.R. § 1.104(c)(2); see also M.P.E.P. § 707). Thus, Applicants' respectfully submit that a *prima facie* case has not been established.

For example, in rejecting claim 1, the Examiner merely cites Asami at "*Abstract, Figs. 1-5B, 8-11, col. 2, lines 58-67, col. 3, lines 1-68, col. 4, lines 20-50, col. 5, lines 1-68, col. 6, lines 3-30*". That is, the Examiner cites nearly all of the Figures of Asami, with the exception of the prior art Figures 6 and 7, and also cites much of the "Detailed Description of the Preferred Embodiments" of Asami.

Therefore, Applicants' respectfully submit that a *prima facie* case has not been established.

Second, notwithstanding the above, Applicants submit that there are features of the claimed invention which clearly are not disclosed or suggested by Asami.

For example, independent claim 1 recites a method of producing a layout pattern of a semiconductor device, including:

> *arranging primitive cells including circuit patterns of constituent elements of said semiconductor device in an element formation area of said semiconductor device; and*
> *arranging at least one fill cell including a diffusion layer and* ***no wiring****, in a vacant area in the element formation area of said semiconductor device that is generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged* (emphasis added).

That is, the claimed method arranges a fill cell which includes a diffusion layer and no wiring. Turning to the specification, it is noted that the specification clearly defines that a "*fill cell*", according to the exemplary aspects of the present invention, includes a construction without gate electrodes (e.g., see specification at page 7, lines 15-18).

As best Applicants can tell, the Examiner appears to be comparing the arrangement of the diffused register regions of Asami with the claimed "*arranging at least one fill cell including a diffusion layer and no wiring*", as recited in independent claim 1.

However, as illustrated in Figure 2, the diffused register regions 23 clearly include wiring (i.e., metal conductors 24)(e.g., see Asami at column 4, lines 2-11).

That is, Asami clearly discloses, with reference to Figure 2, that:

> Each of the second diffused resistor regions is referenced by a numeral 23. Each group of diffused resistor regions 23, for example, three, arranged parallelly (sic) in the column direction is located between two adjacent basic cell lands 21 arranged in the row direction. *Metal conductors* are also illustrated, as wired with the regions 23, for example, from a point .circle.A to a point .circle.B, referenced as numeral 24 with hatchings. Reference numeral 24' represents a particular *metal conductor to be wired* between two adjacent diffused resistor regions only, referred to as a lead conductor hereinafter. These *metal and lead conductors* 24, 24' are connected to diffused resistor regions 23 via contact windows 25 formed in an insulation layer located on

· the surface of the bulk (emphasis added)(see Asami at column 4, lines 2-11).

Thus, Asami clearly does not disclose or suggest at least "*arranging at least one fill cell including a diffusion layer and* ***no wiring****, in a vacant area in the element formation area of said semiconductor device that is generated after said primitive cells associated with all constituent elements of said semiconductor device have been arranged*", as recited by independent claim 1 (emphasis added).

Indeed, Asami does not even contemplate the problem being addressed by the claimed invention, or for that matter, disclose or suggest the claimed method recited in claim 1.

In contrast to Asami, the claimed invention provides a method and device for producing the layout pattern of a semiconductor device that enables uniform planarization of the wafer surface in the CMP processing carried out before forming transistors, and further, that enables a reduction of trouble of the arithmetic processes when producing mask data (e.g., see specification at page 3, lines 14-18).

On the other hand, claim 2 is patentable over Asami by virtue of its dependency from claim 1, as well as for the additional features recited therein.

For example, claim 2 exemplarily defines that the "*fill cells are arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device*" (emphasis added).

According to the claimed invention, since the fill cells can be arranged so as to make the data ratio of the diffusion layer (area ratio of the diffusion layer) fall within a prescribed range, uneven distribution of the diffusion layers is eliminated, whereby a wafer having a uniform surface can be obtained even when CMP is conducted to remove

the insulating film on a wafer having diffusion layers and trenches formed thereon. Further, fill cells according to the exemplary aspects of the claimed invention can be arranged after primitive cells have been arranged and before mask data are made, and the arithmetic processes for making mask data can therefore be reduced (e.g., see specification at page 3, lines 24-27; page 4, lines 1-5; and page 14, lines 2-9).

The Examiner alleges that Asami discloses the fill cells being arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device, citing Figs. 1-5B and 8-11.

However, the Examiner has not identified anywhere in the disclosure in which Asami explicitly discloses such an alleged "uniform distribution", or for that matter, the basis for the Examiner's position that the distribution disclosed in Figures 1-5B and 8-11 teaches or suggests a uniform distribution.

Thus, Asami clearly does not disclose or suggest at least "*fill cells are arranged such that said diffusion layers are uniformly distributed in said element formation area of said semiconductor device*", as recited by claim 2 (emphasis added).

Indeed, Asami does not even contemplate the problem being addressed by the claimed invention, or for that matter, disclose or suggest the claimed method recited in claim 2.

For the foregoing reasons, Asami does not disclose or suggest all of the features of the claimed invention. Therefore, the Examiner is requested to reconsider and withdraw this rejection and to permit claims 1 and 2 to pass to immediate allowance.

B. Claims 4 and 5 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Asami in view of Osono.

The Examiner alleges that the combination of Asami and Osono disclose or suggest all of the features of the claimed invention. Particularly, the Examiner reiterates that Asami shows the features described above.

The Examiner acknowledges, however, that Asami does not specifically show the plurality of types of fill cells having different sizes being identified, grouping and sorting the constituent elements having related operation in order to be arranged in proximity.

However, the Examiner alleges that Osono teaches the plurality of types of fill cells having different sizes being identified, grouping and sorting the constituent elements having related operation in order to be arranged in proximity (citing Osono at the Detailed Description, paragraphs 0011-0044, Operation, paragraphs 0042-0044). Therefore, the Examiner alleges that it would have been obvious to a person of ordinary skill in the art oat the time of the invention to recognize that identifying, grouping and sorting would be infer from Asami reference because is necessary present as evidence Osono et al. in order to reduce the manufacturing cost.

Applicants traverse this rejection for at least the following reasons.

First, Applicants respectfully submit that the Examiner has not properly established a *prima facie* case of obviousness, since the Examiner has merely cited the entire disclosure of Osono (citing Osono at the Detailed Description, paragraphs 0011-0044, Operation, paragraphs 0042-0044), without properly identifying the relevant portions of the Osono reference which the Examiner considers to disclose or suggest the missing features of Asami, or for that matter, that provide the motivation for making such a combination (e.g., see 37 C.F.R. § 1.104(c)(2); see also M.P.E.P. § 707 and M.P.E.P. § 706.02(j)).

That is, the Examiner should set forth in the Office Action the relevant teachings of the prior art relied upon, preferably with reference to the relevant column and page numbers and line numbers where appropriate. It is important for the Examiner to properly communicate the basis for a rejection so that the issues can be identified early and the Applicant can be given fair opportunity to reply (e.g., see M.P.E.P. § 706.02(j)).

Second, notwithstanding the above failure to properly establish a *prima facie* case, Applicants submit that Asami and Osono, either individually or in combination, do not disclose or suggest all of the features of the claimed invention.

Applicants submit that claims 4 and 5 are patentable over Asami and Osono by virtue of their dependency from claim 1, as well as for the additional features recited therein. Indeed, Osono is not even relied upon for the missing features of independent claim 1, as set forth above.

Moreover, the features for which Osono is relied upon are not disclosed or suggested by Osono.

For example, claim 4 recites, *inter alia*, that "a plurality of types of fill cells having different sizes that are each identified by an identifier having the same amount of information are prepared and are arranged in said vacant area in order of size starting from the largest fill cells that can be arranged in said vacant area" (emphasis added).

Osono does not disclose, suggest, or even mention these features. Indeed, the Examiner has not identified any disclosure for such features in the Osono reference.

On the other hand, claim 5 recites, *inter alia*, that the "*constituent elements are grouped such that constituent elements having related operation are sorted into the same group; and said primitive cells associated with constituent elements that belong to the same group are arranged in proximity*" (emphasis added).

Osono does not disclose, suggest, or even mention these features. Indeed, the Examiner has not identified any disclosure for such features in the Osono reference.

Moreover, the Examiner has not identified any disclosure in Asami or Osono for the alleged motivation for combining these features "to reduce the manufacturing cost" (see Office Action at page 5, lines 18-21).

For the foregoing reasons, Applicants respectfully submit that the Examiner has not properly established a *prima facie* case of obviousness, since the Examiner has not identified the relevant portions of the Osono reference which form the basis of the rejection under 35 U.S.C. § 103. That is, the Examiner has not properly identified the relevant portions of the Osono reference which the Examiner considers to disclose or suggest the missing features of Asami, or for that matter, that provide the motivation for making such a combination.

Notwithstanding the above failure to establish a *prima facie* case, Asami and Osono, either individually or in combination, do not disclose or suggest all of the features of the claimed invention. Indeed, the Examiner has not identified any disclosure for such admittedly missing features Asami in the Osono reference.

Therefore, the Examiner is requested to reconsider and withdraw this rejection and to permit claims 4 and 5 to pass to immediate allowance.

C. Claim 6 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Asami in view of Applicants' allegedly Admitted Prior Art (AAPA).

Applicants submit that claim 6 is patentable over Asami and AAPA by virtue of its dependency from claim 1, as well as for the additional features recited therein.

Indeed, the AAPA is not even relied upon for the missing features of independent claim 1, as set forth above.

Therefore, the Examiner is requested to reconsider and withdraw this rejection and to permit claim 6 to pass to immediate allowance.

IV. NEW CLAIMS

New claims 17-29 have been added to provide more varied protection for the present invention.

Claims 17-29 are patentable over the prior art of record for somewhat similar reasons as those set forth above.

The Examiner is requested to permit claims 17-29 to pass to immediate allowance.

V. FORMAL MATTERS

The Office Action objects to the specification because it allegedly has not been checked to the extent necessary to determine the presence of all possible minor errors.

The specification is amended to correct minor errors. Therefore, the Examiner is requested to withdraw this objection to the specification.

VI. CONCLUSION

In view of the foregoing, Applicant submits that claims 1-6 and 17-29, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

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